IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:		Examiner:	Tran, Khanh C.
	Kamilo Feher	Art Unit:	2631
Serial No.:	**09/370,360**	Class-Subclass:	375-259000
Filed:	**August 9, 1999**	Atty Docket No.:	A-66732-2/RMA
Title:	**Spectrally Efficient FQPSK, FGMSK, and FQAM for Enhanced Performance CDMA, TDMA, GSM, OFDM, and Other Systems**		

CERTIFICATE OF FACSIMILE TRANSMISSION
I hereby certify that this correspondence is being forwarded by facsimile to (703) 308-6642 to Mr. Derrick Rich, Office of Publications, Assistant Commissioner for Patents, Washington, DC 20231 on September 11, 2002.

By: Karena J Moy Brown
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Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

Sir:

In response to the telephonic communication from the Publications Branch on 10 September 2002, applicant provides the requested brief description of figures 10b, 11b, 11c, 13b, and 13c. This information is submitted in the form of an amendment and introduces no new matter. Please amend the application as follows:

IN THE BRIEF DESCRIPTION OF DRAWINGS

Delete the paragraphs beginning at page 13, line 23 through page 14, line 1, and insert the following paragraphs:

FIG. 10b shows the implementation architecture of an alternative XCSI with PL single or multiple XCSI and/or Peak Limiter (PL) processor.

FIG. 11a illustrates NRZ signal and shaped Feher Return-to-Zero (FRZ) signal patterns and an embodiment having TCS response and cascade LR filters in which the LR filter is implemented with digital IIR and/or FIR filters.

FIG. 11b shows a pre-processor based architecture of a BRA system with single or multiple Signal Element (SE) storage and/or inverter and of single or multiple D/A based architecture having selectable 1 to N filter channel banks.

FIG. 11c shows an implementation of a Bit Rate Agile (BRA) pre-processor with single or multiple wavelets Signal Element (SE) storage and/or inverter and of filtered SE and ACM processors is illustrated.

FIG. 12a shows analog implementation components for cross-correlated and/or TCS-filtered data patterns and signals for bit rate agile and for high bit rate applications are shown.

FIG. 12b shows an analog BRA baseband implementation alternative of a TCS response processor for cross-correlated or not cross-correlated I and Q signals with selection or combined cascaded LR filter embodiment of this invention.

FIG. 13a is a mixed analog and digital circuit implementation alternative of this cross-correlated TCS response processor in cascade with LR filters.

FIG. 13b shows an other cross-correlated alternative implemented with a combination and/or selection of analog and digital circuits.

FIG. 13c shows a detailed implementation structure for one of the channels (I or Q) of a TCS response processor in cascade with a LR filter. In some embodiments the TCS processor contains cross-correlation between the I and Q channels while in other implementations there is no cross-correlation between the TCS response and cascaded LR filtered signals.